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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/679,355	10/07/2003	Yasuhiro Araki	402813	3865

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EXAMINER	
PAREKH, NITIN	

ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 07/13/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/679,355	ARAKI, YASUHIRO	
	Examiner	Art Unit	
	Nitin Parekh	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 October 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *07 October 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 2.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The Information Disclosure Statement filed on 10/07/03 has been considered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

3. Claim 1 is rejected under 35 U.S.C. 102(a) as being anticipated by Yang et al. (US Pat. Application Pub. 2002/0105088).

Regarding claim 1, Yang et al. disclose a semiconductor device comprising:

- a semiconductor substrate (300 in Fig. 3G)
- a first interlayer insulating/dielectric film (IDL- 310 in Fig. 3G) formed on the semiconductor substrate and having first contact holes (see 316 in Fig. 3B)
- first contact plugs (see 318b/320 in Fig. 3D and 3G) each having a portion buried in one of the first contact holes (see 318b in Fig. 3G) and a portion protruded (see 320 in Fig. 3D and 3G) from the surface of the first interlayer film
- sidewalls/spacers (see 326 in Fig. 3E and 3G) formed on the sides of the protruded portions of the first contact plugs

- a second IDL (328 in Fig. 3G) formed on the first interlayer insulating film, the first contact plugs, and the sidewalls, and having second contact holes (not numerically referenced- see hole having a second plug 340 in Fig. 3G), and
- the second contact plugs (340b in Fig. 3G) formed in the second contact holes and connected to the first contact plugs

(Fig. 3A-3G; sections 0043-0058).

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

5. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US Pat. Application Pub. 2002/0105088) in view of Koh et al. (US Pat. 5627095).

Regarding claim 2, Yang et al. teach substantially the entire claimed structure as applied to claim 1 above, wherein Yang et al. teach conventional gate electrodes being formed having active regions/source-drain junctions in the vicinity (see 306, 308, etc. in

Fig. 3G; section 0044) on the semiconductor substrate wherein the first contact plugs are connected to the active regions/source-drain junctions, but Yang et al. fail to teach the lateral width of the sidewalls being larger than the distance between the first contact plugs and the gate electrodes.

Koh et al. teach a variety of spacer/sidewall configurations (Fig. 4D-5 and 2A-G) in a memory cell where a lateral width of the sidewalls is larger than a spacing (S)/distance between the first contact plugs and the gate electrodes (see the width of spacer 39 versus the spacing S in Fig. 4H and 5) to provide the desired alignment margin, over-etch protection and to prevent shorting (Col. 6 and 7; Col. 7, lines 26-65).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the lateral width of the sidewalls being larger than the distance between the first contact plugs and the gate electrodes as taught by Koh et al. so that the desired alignment margin and the over-etch protection can be achieved and the reliability can be improved in Yang et al's device.

6. Claim 4 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ryou (US Pat. 5492851) in view of Stinnett et al. (US Pat. 6355557).

Regarding claim 4, Ryou discloses semiconductor device comprising:

- a semiconductor substrate (1 in Fig. 2E)

- a first interlayer insulating film (IIF)/composite IIF (see 7/12/13 in Fig. 2E) formed on the semiconductor substrate and having first contact holes (not numerically referenced- see the hole having conductive plug 13 in Fig. 2C and 2E)
- first conduction layer/electrode plugs/contact plugs (CL/CP 13 in Fig. 2E) formed in the first contact holes and each having a funnel shape at the top (see 13 in Fig. E)
- the first CL/CP having portions buried in the first contact holes and top portions protruded from the surface of the first IIF/composite IIF (see top portion of 13 above IIF 12 in Fig. 2E)
- a second IIF (14 in Fig. 2E) formed on the first IIF and the first contact plugs and having second contact holes (not numerically referenced- see the hole having conductive plug 21 above the plug 13 in Fig. 2E), and
- second conduction layer/electrode plugs/contact plugs (21 in Fig. 2E) formed in the second contact holes and connected to the first contact plugs

(Fig. 2E; Fig. 1-2E; Col. 2, line 45- Col. 4, line 15).

Ryou fails to teach the contact holes in the IIF having a downwardly convex funnel shape.

Stinnett et al. teach a variety of contact hole configurations (see Fig. 1 and 7) where the contact holes (see 24/36 and 16 in Fig. 7 and 1 respectively) in the IIF having

a wine glass/downwardly convex funnel shape to provide an improved metal filling and optimized etching (Col. 1-4).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the contact holes in the IIF having a downwardly convex funnel shape as taught by Stinnett et al. so that the metal fill can be improved and the etch process can be optimized in Ryou's device.

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yang et al. (US Pat. Application Pub. 2002/0105088) and Koh et al. (US Pat. 5627095) as applied to claims 1 and 2 above, and further in view of Chu (US Pat. 5783471).

Regarding claim 3, Yang et al. and Koh et al. teach substantially the entire claimed structure as applied to claims 1 and 2 above, except the first contact plugs comprise memory cells of flash memories, and each of the gate electrodes comprise the control gate and the floating gate of the memory cells.

Chu teaches conventional memory cells including flash memories (see Fig. 1-3V) having source/drain regions where gate electrodes comprise the control gate and the floating gate of the memory cells (see 301, 302, etc. in Fig. 1-3V; Col. 1-5).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the memory cells having flash memories and each of the gate electrodes comprise the control gate and the floating gate of the memory cells

as taught by Chu so that the desired functionality and circuit requirements/applications can be achieved in Koh et al. and Yang et al's device.

8. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ryou (US Pat. 5492851) and Stinnett et al. (US Pat. 6355557) as applied to claim 4 above, and further in view of Yang et al. (US Pat. Application Pub. 2002/0105088).

Regarding claim 5, Ryou and Stinnett et al. teach substantially the entire claimed structure as applied to claim 4 above, except the extruded portions having sidewalls on the sides.

Yang et al. disclose the semiconductor device comprising sidewalls/spacers (see 326 in Fig. 3E and 3G) formed on the sides of the protruded portions of the first contact plugs to provide the desired etch stop and over-etch protection (0053).

It would have been obvious to a person of ordinary skill in the art at the time the invention was made to incorporate the extruded portions having sidewalls on the sides as taught by Yang et al. so that the desired etch protection and alignment can be achieved in Stinnett et al. and Ryou's device.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 571-272-1663. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Eddie Lee can be reached on 571-272-1732. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9318.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956

NP
07-10-04

Nitin Parekh

PATENT EXAMINER
TECHNOLOGY CENTER 2800